



**UNIVERSITI PUTRA MALAYSIA**

**DESIGN OF HIGH-SPEED MULTIPLIER WITH OPTIMISED BUILT-  
INSELF-TEST**

**WAN ZUHA WAN HASAN**

**FK 2000 14**

**DESIGN OF HIGH-SPEED MULTIPLIER WITH OPTIMISED BUILT-IN-  
SELF-TEST**

**By**

**WAN ZUHA WAN HASAN**

**Thesis Submitted in Fulfilment of the Requirements for the  
Degree of Master of Science in the Faculty of Engineering  
Universiti Putra Malaysia**

**March 2000**



**I dedicate this thesis to my family and Hasliza Hashim**

**Abstract of thesis presented to the Senate of Universiti Putra Malaysia  
in fulfilment of the requirements for the degree of Master of Science.**

**DESIGN OF HIGH-SPEED MULTIPLIER WITH OPTIMISED  
BUILT-IN SELF-TEST**

**By**

**WAN ZUHA BIN WAN HASAN**

**March 2000**

**Chairman: Bambang Sunaryo Suparjo, Ph.D**

**Faculty: Engineering**

Current trend in Integrated Circuits (IC) implementation such as System-on-Chip has contributed significant advantages in electronic product features such as high circuit performance with high number of functions, small physical area and high reliability. Since the development of System-on-Chip, which is based on integrating subsystems supplied by various Intellectual Properties (IP) Block vendors, the required design time is shorter when compared to that of full-custom IC implementation.

However, testing each internal subsystems using the common scan-path method where test data are generated and analyzed externally is considered too time consuming when the number of subsystems is high. Therefore, by including Built-In-Self-Test (BIST) facility into each subsystem is considered a good solution. Commonly, BIST structure is based on random test data generation from a Linear Feedback Shift Register (LFSR) due to its simple, small and economical circuit structure. Since the number of subsystems in an IC chip is going to be increased from

time to time, improvement on the BIST approach is required to provide shorter testing time while keeping the good features of LFSR.

For this reason, development of test pattern for BIST based on combination of LFSR and deterministic approach could provide one of the solutions to reduce the testing time. In this research, the possibility of combining LFSR features and deterministic test pattern was carried out. A parallel high-speed multiplier considered as one of the demanding subsystems was chosen to verify the proposed BIST performance. Results show that the testing time (with 100% fault coverage) was reduced significantly when compared to the testing time taken for the BIST that was totally based on random test data generation.

One of the reasons for this achievement is only one basic cell of the multiplier is required to determine the test pattern by considering the data flow from one cell to another. Identical test data can then be applied to both multiplier inputs simultaneously. This is the significant finding of the research. Further works based on the finding are also identified.

**Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia  
sebagai memenuhi keperluan untuk Ijazah Master Sains**

**REKABENTUK PENDARAB PANTAS DENGAN PENGOPTIMUMAN  
‘BUILT-IN SELF-TEST’**

**Oleh**

**WAN ZUHA BIN WAN HASAN**

**Mac 2000**

**Pengerusi: Bambang Sunaryo Suparjo, Ph.D**

**Fakulti: Kejuruteraan**

Kaedah terkini dalam implimetasi Litar Kamilan seperti “System-on-Chip” telah memberikan faedah-faedah yang penting terhadap barangan elektronik seperti mutukerja litar yang tinggi dengan bilangan fungsi yang banyak, keluasan fizikal yang kecil dan ketahanan yang tinggi. Memandangkan pembangunan “System-on-Chip” berdasarkan penggabungan subsistem-subsistem yang dibekalkan oleh vendor-vendor blok “Intellectual Properties (IP)”, masa yang diperlukan untuk rekabentuk adalah pendek jika dibandingkan dengan implementasi litar kamilan secara “full-custom”.

Walaupun demikian, pengujian untuk setiap subsistem dalaman menggunakan kaedah biasa “scan-path” di mana data pengujian dijanakan dan dianalisis dari luaran akan memerlukan masa yang lama memandangkan bilangan subsistem yang banyak. Oleh itu, dengan menyediakan “Built-in Self-Test (BIST)” dalam setiap subsistem boleh dikatakan satu penyelesaian yang baik. Pada kebiasaan, struktur BIST adalah berdasarkan penjanaan data pengujian secara rawak dari “Linear Feedback Shift Register (LFSR)” disebabkan oleh stuktur litarnya yang mudah, kecil dan ekonomi.

Memandangkan bilangan subsistem dalam cip litar kamilan akan bertambah dari masa ke masa, pembaharuan terhadap kaedah BIST adalah perlu supaya masa pengujian akan menjadi lebih pendek disamping mengekalkan penggunaan LFSR. Atas alasan ini, pembangunan corak data pengujian untuk BIST berdasarkan gabungan LFSR dan kaedah “deterministic” adalah mungkin boleh menyediakan salah satu penyelesaian untuk memendekkan masa pengujian. Dalam penyelidikan ini, kajian terhadap kemungkinan menggabungkan LFSR dan corak pengujian “deterministic” telah dilakukan. Pendarab pantas secara selari yang dianggap sebagai salah satu subsistem yang banyak diperlukan adalah dipilih bagi menentukan mutukerja BIST yang dicadangkan. Keputusan penyelidikan menunjukkan masa pengujian (dengan “fault coverage” 100%) telah dipendekkan berbanding dengan masa pengujian yang diambil untuk BIST yang hanya berdasarkan penjanaan data pengujian secara rawak.

Salah satu alasan atas pencapaian ini adalah hanya satu sel dalam pendarab tersebut diperlukan untuk menentukan corak pengujian dengan mengambilkira aliran data dari satu sel kepada yang lain. Data pengujian yang sama kemudian boleh dikenakan kepada kedua-dua input pendarab secara serentak. Ini adalah hasil utama dari penyelidikan ini. Kerja-kerja akan datang berdasarkan hasil yang didapati telah juga dikenalpasti.

## **ACKNOWLEDGEMENTS**

I would like to thank my supervisor, Dr Bambang Sunaryo Surpajo, Head, Department of Electrical and Electronic Engineering, UPM who patiently advised and assisted me to finish my thesis at the optimum period and I deeply indebted to him for his useful suggestion and encouragement. His constant help and encouragement are very much appreciated. Also, I would like to thank Dr Mohd Rais Ahmad and Mr Rahman Wagiran whom has supervision had really supported and encouraged me to continue in my project. My sincere gratitude also to the friends especially Nasri Sulaiman and Hashim Nizam for his consultants and staff of the Faculty of Engineering, University of Putra for assistance rendered.

Thanks to my family who indeed support and taught me the significant meaning of patience and accuracy in dealing with hard work and facing difficulties.



I certify that an Examination Committee met on 22<sup>nd</sup> March 2000 to conduct the final examination of Wan Zuha Wan Hasan on his Master of Science thesis entitled "Design of High Speed Multiplier with Optimised Built-in Self-test" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

**BARKAWI SAHARI, Ph.D.**

Associate Professor  
Faculty of Engineering  
Universiti Putra Malaysia  
(Chairman)

**BAMBANG SUNARYO SUPARJO, Ph.D.**

Faculty of Engineering  
Universiti Putra Malaysia  
(Member)

**MOHD RAIS AHMAD, Ph.D.**

Manager  
Microelectronics Laboratory  
Mimos Berhad  
(Member)

**RAHMAN WAGIRAN, M.Sc.**

Faculty of Engineering  
Universiti Putra Malaysia  
(Member)



-----  
**MOHD GHAZALI MOHAYIDIN, Ph.D.**  
Professor / Deputy Dean of Graduate School  
Universiti Putra Malaysia

Date     **17 MAY 2000**

This thesis was submitted to the Senate of Universiti Putra Malaysia and was accepted as fulfilment of the requirements for the degree of Master of Science.




**KAMIS AWANG, Ph.D.**

Associate Professor / Dean of Graduate School  
Universiti Putra Malaysia

Date: **11 MAY 2000**

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

  
-----  
WAN ZUHA WAN HASAN  
Date: 10/5/2000

## TABLE OF CONTENTS

	Page
DEDICATION .....	2
ABSTRACT .....	3
ABSTRAK .....	5
ACKNOWLEDGEMENTS .....	7
APPROVAL SHEETS .....	8
DECLARATION FORM .....	10
LIST OF FIGURES .....	13
LIST OF TABLES .....	15
LIST OF ABBREVIATIONS .....	16
<b>CHAPTER</b>	
<b>I INTRODUCTION .....</b>	<b>18</b>
Current Trend in Integrated Circuit Implementation .....	18
Built-In-Self-Test (BIST) Features .....	19
Objective .....	21
Thesis Organisation .....	21
 <b>II LITERATURE REVIEW .....</b>	 <b>22</b>
IC as a Current Approach .....	22
The Role of Multiplier in Signal Processing .....	23
Multiplier Architecture .....	23
Parallel Multiplier with Ripple Carry (PMRC) .....	28
Testing Technique .....	31
Test Pattern Generation .....	31
Random Pattern and LFSR .....	33
Random Testing .....	34
Signature Analysis .....	36
Application Example .....	37
Data Compression Methods .....	42
Design for Testability .....	42
Testing Level Sensitive Scan Design (LSSD) .....	43
Scan Path .....	44
Scan or Set Logic .....	45
Random Access Scan .....	45
Boundry Scan .....	46
On-Chip Hardware for Real-time Test Generation .....	46
Built-in Logic Block Observation (BILBO) .....	47
Built-in Evaluation and Self-test (BEST) .....	48
Self-testing and Built-in Test .....	48

Autonomous Test .....	49
The Need for DFT/ BIST .....	49
Discussion .....	50
<b>III DESIGN AND ANALYSIS OF MULTIPLIERS .....</b>	<b>52</b>
Methodology .....	52
Design and Analysis of Serial Multiplier .....	53
Design and Analysis of Parallel Multiplier .....	56
Analysis Result .....	60
<b>IV RESULT and DISCUSSION .....</b>	<b>62</b>
Multiplier Testing .....	62
Scan Path Approach .....	62
Built-in Self-test Approach .....	65
BIST Flow Process .....	67
Linear Feedback Shift Register (LFSR) .....	68
Proposed Test Approach .....	69
BIST Design for Parallel Multiplier with Ripple Carry (PMRC) .....	69
Test Pattern Generation (TPG) and LFSR .....	70
Deterministic Testing .....	70
Design of LFSR .....	74
Signature Analysis and Design 8-bit Comparator .....	76
Simulation Process and Result .....	81
General Discussion .....	85
Advantages of BIST .....	87
<b>V CONCLUSION .....</b>	<b>88</b>
<b>REFERENCES .....</b>	<b>91</b>
<b>VITA .....</b>	<b>94</b>

## LIST OF FIGURES

Figure	Page
1      4-bit Multiplication .....	23
2      4-bit Multiplication with Partial Products .....	23
3      Adder Circuit .....	26
4      n-bit Ripple Carry Adder .....	26
5      Basic Building Block for PMRC .....	28
6      Interconnection of 16 Basic Building Blocks for Parallel Multiplier	29
7      Linear Feedback Shift Register (LFSR) Circuit .....	33
8      Principle of Random Testing .....	35
9      Example of Logic Circuit for Test Generation .....	37
10     Block Diagram of Serial Multiplier .....	54
11     Schematic Diagram of Serial Multiplier .....	55
12     Basic Cell of Parallel Multiplier .....	57
13     Schematic Diagram of 4-bit Parallel Multiplier .....	58
14     Output of 4-bit Parallel Multiplier .....	59
15     Scan Path Technique for PMRC .....	63
16     BIST Architecture for 4-bit Parallel Multiplier .....	65
17     BIST Process Flow .....	67
18     Basic Cell of 4-bit PMRC .....	70
19     Schematic Diagram of LFSR .....	75
20     Schematic Diagram of Signature Analysis for PMRC .....	77



21	Signature Output for PMRC .....	78
22	Schematic Diagram of 8-bit Comparator .....	79
23	Output of 8-bit Comparator .....	80
24	Schematic Diagram of BIST for PMRC .....	83
25	Output of BIST for PMRC .....	84

## LIST OF TABLES

Table	page
1 Truth Table for Adders .....	25
2 Truth Table for NAND, AND, and OR Gates .....	39
3 Test Vectors Selection Process .....	40
4 Selected Test Vectors to Cover All the Stuck-at-faults .....	40
5 Sequences of Operation Refer to Figure 14 .....	60
6 Criteria for 4-bit Multiplier .....	61
7 List of Stuck-at-faults and Test Vectors of 4-bit PMRC .....	71
8 The Selection Test Vectors for PMRC .....	71
9 Propagation Node for Fault-Free Output .....	72
10 Test Pattern for PMRC .....	75
11 Signature Output of PMRC .....	79
12 Initial Values of LFSR .....	86



## LIST OF ABBREVIATIONS

ATE	- Autonomous Test Equipment
ATPG	- Autonomous Test Pattern Generation
BIST	- Built-in Self-Test
BEST	- Built-in Evaluation and Self-Test
BILBO	- Built-in Logic Block Observation
C	- Carry
Cps	- Center Points
CUT	- Circuit Under Test
DFT	- Design For Testability
DUT	- Device Under Test
ECL	- Emitter Couple Logic
IC	- Integrated Circuit
I/O	- Input/Output
LFSR	- Linear Feedback Shift Register
LSI	- Large Scale Integration
LSSD	- Level Sensitive Scan Design
MISR	- Multiple Input Signature Register
MSI	- Medium Scale Integration
ORA	- Output Response Analysis
PMRC	- Parallel Multiplier With Ripple Carry

PMCLA	- Parallel Multiplier With Carry Lookahead
P	- Propagation
Pis	- Original (input)
Pos	- Destination (output)
PO	- Primary Output
ROM	- Read Only Memory
S-a-0	- Stuck-at-0
S-a-1	- Stuck-at-1
S-a-Fault	- Stuck-at-Fault
TPG	- Test Pattern Generation
TTL	- Transistor-Transistor Logic
UUT	- Unit Under Test
VLSI	- Very Large Scale Integration

# **CHAPTER 1**

## **INTRODUCTION**

### **Current Trend in Integrated Circuits Implementation**

The steady down scaling of microelectronic devices has made electronic companies to continually produce low cost products that capable to provide more functions, higher performance and higher reliability. Many electronic sub-systems or modules such as microprocessor, analog-digital converters, memories and interface circuits that previously been packaged individually are now being able to be integrated onto a single silicon chip to form a specific system. Such implementation is known as System-on-Chip. This approach can provide many advantages in terms of physical size, cost, performance and reliability.

The design and implementation processes of System-on-Chip are not as critical as testing the chip after the completion of manufacturing processes since there are many design automation software available in the market. For System-on-Chip implementation, testing operations can be costly and time consuming if consideration on embedding on-chip testing facilities is neglected during the design stage. This is true when the circuit density, functional and complexity are increased, testing the overall chip based on ad-hoc method is almost impossible to detect all the predefined

circuit faults within the allowable testing period. Although the chip is accommodated by normal scan path testing facility i.e. each input/output of subsystem boundaries can be accessed via a shift register chain, managing the transportation of test data stimulus and test data results can become complex [1]. This is because the number of internal subsystems is large while the number of externally accessible test points is small. Hence, large size of test circuits and long test time are needed to access each internal individual sub-system using external test data generator and test results analyzer. Any factors that affect the testing cost will increase the price of the product. In addition, the longer testing time will delay the product time-to-market.

### **Built-In-Self-Test (BIST) Features**

Presently, there has been an increasingly interest in embedding Built-In-Self-Test (BIST) facility onto large and complex IC chips. The good features of BIST include short test operation time and the IC can be tested based on normal or operating clock frequency since the test data generator and test results analyzers are built internally i.e. in the IC. These two features are suitable for on-line testing purposes. Most of the real-time controller ICs used in automobiles and airplanes has already been designed with BIST facility to accommodate on-line testing or real-time monitoring [2]. In this case, system failures can be detected immediately so that the system will be brought back into normal operation quickly. It can provide low down time that is required most by customers. Since modern control systems often include microprocessor or Digital Signal Processing (DSP) chips that might be sensitive to

vibration or stress environment, the involvement of BIST in monitoring the system operation and performance is considered important.

Several methods of BIST have been proposed for general and specific IC applications. However, continuous development is necessary to prepare for the future trend in System-On-Chip implementation. In System-on-Chip development, designer can select IC subsystems from several vendors in the form of software such as in hardware-description-language (HDL), gate or transistor level circuit netlist and, IC mask layout. During the development process, subsystems with BIST facility simplify the effort in providing test data path management system as well as optimizing the overall circuit size.

There are two main criteria need to be considered in developing internal IC test system; performance or efficiency and overhead. An efficient test system will detect most or all the predefined faults within allowable test period. The inclusion of test control circuitry in the IC should not give significant impact on the overall IC implementation overhead because it can influence the product price in the market. In common BIST, the test data generator is based on random data generation. Although this type of generator can be designed by a small circuit i.e. using Linear-Feedback-Shift-Register (LFSR), the length of test sequence can be long to cover the required predefined faults since some of the data are not being used to detect the faults. For this reason, study on the possibility of combining BIST approach with conventional

deterministic test pattern generation approach was carried out to propose a high performance BIST

### **Objective**

The objective of this thesis is to design a high-speed multiplier with optimised Built-in Self-test

### **Thesis Organisation**

This thesis describes the development of BIST based on deterministic test pattern generation (and random pattern generation) using LFSR. It contains 6 chapters. The next chapter reviews the present and past works on fault detection and Design-For-Testability (DFT) where the most critical problem in generating test pattern and development of DFT circuit specifically on BIST are identified. The fundamental theory of BIST is described in Chapter 3. Multiplier was chosen as a sample of IC subsystem due to its widely used in most Digital-Signal-Processing (DSP) chip. Basic operation of multiplier is also included in Chapter 3. Chapter 4 describes the development of proposed BIST together with its result and discussion. Finally, the works are concluded in Chapter 5.

## **CHAPTER 2**

### **LITERATURE REVIEW**

#### **IC as a Current Approach**

High complexity of modern digital signal processing system while increasing demand for a short time-to-market is one of the current challenge of today's VLSI designers. An improvement in silicon technology is the enabler to combine more and more circuit functions on a single chip. These circuit functions are implemented by using various subsystems supplied by vendors that are available in commercial Electronic Design Automation (EDA). Sometime the said subsystems are known as Intellectual Property (IP) blocks that play an important role in the device. Systems-on-Chip contribute the following advantages compared to that of the well-established Systems-on-a-board.

- lower cost for consumer applications (high volume)
- higher inter-block communication bandwidth (shorter delays, no pin-limit)
- higher flexibility because of programmable components
- low-power consumption due to smaller device size

Computer processor speeds have increased dramatically. As the original equipment manufacturers (OEMs) introduce computers with faster and more powerful CPUs, the memory industry is developing semiconductor technology that allows

system memory to exchange data with today's high performance CPUs more quickly and efficiently. With synchronous operations, the processor knows when operations are going to be completed and data is going to be available. Therefore, the processor can perform other operations and does not have to wait for the memory to locate the address and read or write the data [3]

### **The Role of Multiplier in Signal Processing**

Multiplier is suitable for high performance DSP applications such as in pattern recognition. There are three famous multiplication techniques; Wallace trees, Booth encoding and binary tree vector merging addition. Results indicated a delay reduction of 10-20% is achieved based on such techniques compared to that of parallel multiplier ripple carry technique. In addition, power and area consumption are also reduced when the device size reduces (traditional)[4].

### **Multiplier architecture**

A Multiplier multiplies two binary numbers or operands; multiplicand and multiplier. An example of operation is shown in Figure 1



